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SILICON CLOCKS ANNOUNCES NEW TIMING PRODUCT LINE

Novel Products Based on Company's Proprietary SmartPLL™ Technology Platform

Fremont, CA – January 20, 2009 – Silicon Clocks, a leading developer of custom semiconductor timing solutions, today released its first high-performance, configurable J-Series™ Precision Frequency Synthesizers to the market. Based upon the company's SmartPLL™ technology platform, the J-Series™ products exhibit lower jitter over a wide range of temperatures and supply voltages at reduced cost and power consumption relative to competing solutions. The J-Series™ products support most high-speed serial communications standards, including: Ethernet, 10G, 12G, XAUI, SATA, FibreChannel, SDH SONET, PCI-e, and SRIO.

The J-Series™ is an attractive alternative for markets traditionally served by a myriad of expensive, bulky, high-power, solutions requiring expensive crystal or SAW components. The J-Series™ delivers SONET-level performance at a price point, flexibility, power, and form factor that makes it attractive for cost-constrained, high-volume applications.

The J-Series™ synthesizer family consists of two devices today, featuring a single precision clock output in LVPECL at differing output frequencies. Additional products will be added shortly with different I/O types (LVDS) based upon required output frequencies. Full industrial temperature range compliance (-40 °C to +85 °C) over both 3.3 V and 2.5 V ranges, coupled with a very low noise and low power design, yield accuracies of <1 ps rms jitter (600 fs is typical) and result in very low phase noise between 12 kHz and 20 MHz. Silicon Clocks' SmartPLL™ architecture exhibits a ±0 ppm periodic error contribution for the PLL, thus providing an extremely stable output frequency with excellent duty cycle (48/52 worst case) and very low dynamic power consumption (<80 mA).

The outputs are robust with fast edges (<500 ps), and are capable of driving one or two transmission lines, providing a precision clock output that can be configured for one of 23 supported frequencies ranging from 62.5 MHz up to 670 MHz. The J-Series products are available in wafer form, tested dice or packaged in a small form factor 3 × 3 mm QFN. A fully integrated Crystal Oscillator circuit, complete with internal trim/loading caps, yields a low device count, while configuration pins allow for setting the output frequency.

"We have worked toward a best-in-class CMOS implementation for a configurable Frequency Synthesizer that can address a wide range of High Speed Serial Data (HSSD) standards," said Silicon Clocks CEO Didier Lacroix. "Our SmartPLL™ technology platform yields high-performance VCOs and PLLs, providing our customers with precision timing solutions that meet and exceed expectations for cost, performance and accuracy. As a developer of custom timing solutions, focused on new product development, we worked closely with our partners to ensure that our products have a real market appeal and are actively sold through their existing sales channels."

Mark Sherwood, Principal Associate at CS &A LLC, a market analyst and consultant focused on Semiconductor Timing, said: "The J-series™ has achieved and demonstrated high stability and excellent accuracy making it competitive for Physical Layer and MAC timing solutions – Host Bus adapters, Network Interface Cards, Access Points, Routers, Switches, Hubs and more can benefit from the ultra low noise, low power, and small form factor.

This family of products is competitive with solutions from IDT, Maxim, Analog Devices, and provides for a path to lower cost, high performance XO solutions.”

About Silicon Clocks

Headquartered in Fremont, CA, Silicon Clocks is a custom product development and licensing company focused upon high performance semiconductor timing and sensor designs and its patented CMEMS™ technology. Silicon Clocks is backed by leading venture investors, including Tallwood Venture Capital, Charles River Ventures, Formative Ventures and Lux Capital. For more information, visit: www.siliconclocks.com

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